Pre.	S.Uchida	Rev	A	H. Harada
Apr.	M.Tabata 23-Oct-'02			M. Tabata 14-Jan.-'03

Notice : This is not a final specification. Some parametric limits are subject to change.

CM400DY-24NF

- Ic 400A
- V_{CES} 1200V
- Insulated Type
- 2-elements in a pack

APPLICATION

General purpose inverters & Servo controls,etc

ABSOLUTE MAXIMUM RATINGS (T_j = 25 °C)

Symbol	Item	Conditions	Ratings	Units
V_{CES}	Collector-emitter voltage	G-E Short	1200	V
V_{GES}	Gate-emitter voltage	C-E Short	±20	V
I_C	Collector current	Tc= 25 °C	400	A
I_{CM}		Pulse ②	800	
I_E ①	Emitter current	Tc= 25 °C	400	A
I_{EM} ①		Pulse ②	800	
Pc ③	Maximum collector dissipation	Tc= 25 °C	1470	W
Tj	Junction temperature		−40~+150	°C
Tstg	Storage temperature		−40~+125	°C
Viso	Isolation voltage	Main terminal to base plate,AC 1 min.	2500	V
—	Torque strength	Main terminal M6	3.5 ~ 4.5	N·m
—	Torque strength	Mounting holes M6	3.5 ~ 4.5	N·m
—	Weight	Typical value	580	g

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Units	
I_{CES}	Collector cutoff current	$V_{CE}=V_{CES}, V_{GE}=$ 0V		–	–	1	mA	
$V_{GE(th)}$	Gate-emitter threshold voltage	I_C=40mA, $V_{CE}=$ 10V		6	7	8	V	
I_{GES}	Gate leakage current	$V_{GE}=V_{GES}$, $V_{CE}=$ 0V		–	–	0.5	μA	
$V_{CE(sat)}$	Collector to emitter saturation voltage	$T_j=$ 25 °C	I_C = 400A	–	1.8	2.5	V	
		$T_j=$ 125 °C	$V_{GE}=$ 15V	–	2.0	–		
Cies	Input capacitance	$V_{CE}=$ 10V		–	–	94	nF	
Coes	Output capacitance	$V_{GE}=$ 0V		–	–	8		
Cres	Reverse transfer capacitance			–	–	1.8		
Q_G	Total gate charge	V_{CC}=600V, Ic=400A, V_{GE}=15V		–	2700	–	nC	
td(on)	Turn-on delay time	V_{CC}=600V, Ic=400A		–	–	600	ns	A
tr	Turn-on rise time	$V_{GE1}=V_{GE2}$=15V		–	–	160		A
td(off)	Turn-off delay time	$R_G=$ 0.73Ω, Inductive load		–	–	700		A
tf	Turn-off fall time	switching operation		–	–	350		
trr ①	Reverse recovery time	I_E=400A		–	–	250	ns	
Qrr ①	Reverse recovery charge			–	16	–	μC	A
V_{EC} ①	Emitter-collector voltage	I_E=400A, $V_{GE}=$ 0V		–	–	3.2	V	
Rth(j-c)Q	Thermal resistance*1	IGBT part (1/2 module)		–	–	0.085	°C/W	
Rth(j-c)R		FWDi part(1/2 module)		–	–	0.15		
Rth(c-f)	Contact thermal resistance	Case to fin, Thermal compound Applied (1/2module) *2		–	0.02	–		
Rth(j-c')Q	Thermal resistance	Tc measured point is just under the chips		–	–	0.034*3		
RG	External gate resistance			0.73	–	7.3	Ω	

*1: Tc measured point is shown in page OUTLINE DRAWING.
*2: Typical value is measured by using Shin-etsu Silicone "G-746".
*3: If you use this value , Rth(f-a) should be measured just under the chips.

① I_E, V_{EC}, trr, Qrr & die/dt represent characteristics of the anti-parallel, emitter to collector free-wheel diode (FWDi).

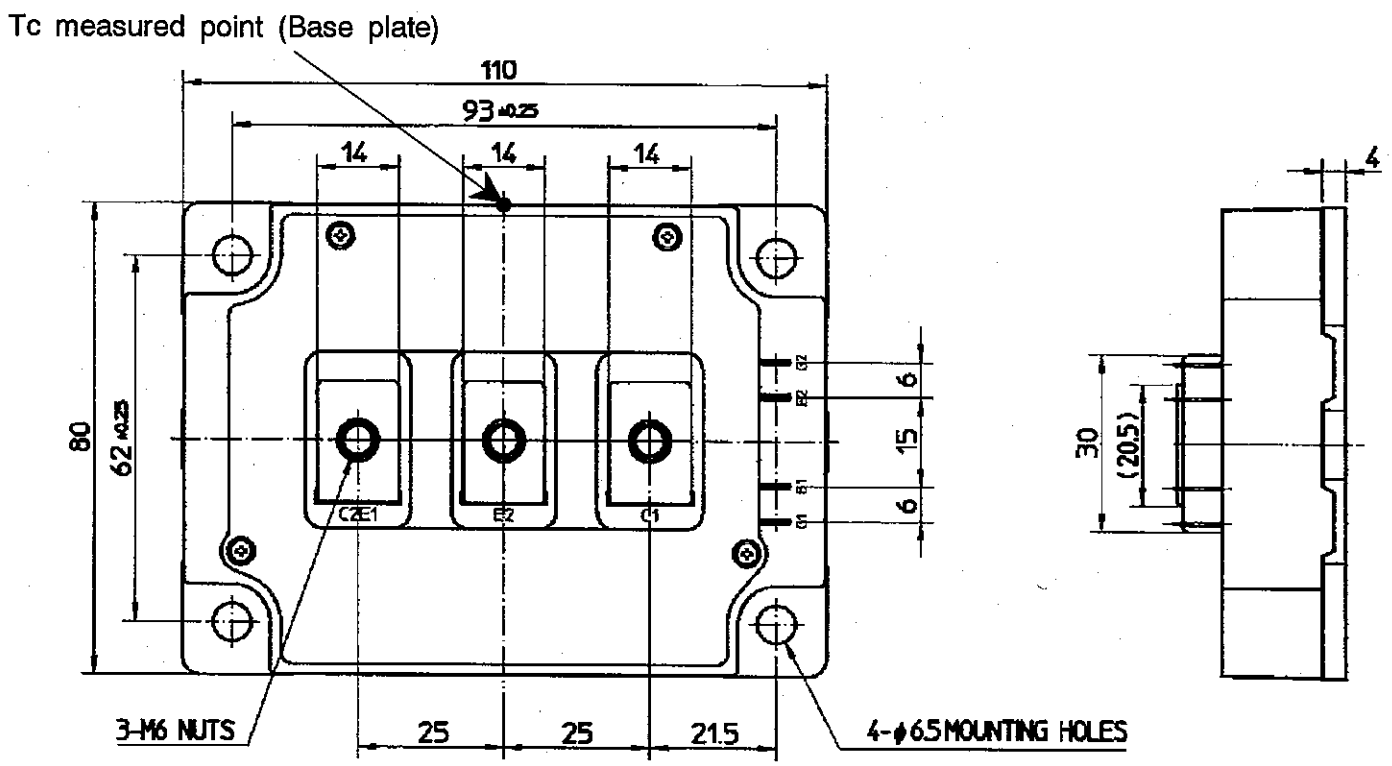
② Pulse width and repetition rate should be such that the device junction temp.(T_j) dose not exceed Tjmax rating.

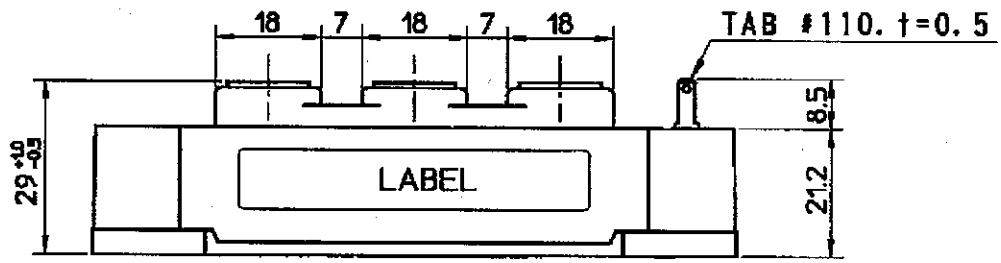
③ Junction temperature (T_j) should not increase beyond 150°C.

④ Pulse width and repetition rate should be such as to cause neglible temperature rise.

OUTLINE DRAWING

Dimensions in mm





CIRCUIT DIAGRAM